

Description

DELAY CIRCUITS AND RELATED APPARATUS FOR EXTENDING DELAY TIME BY ACTIVE FEEDBACK ELEMENTS

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to delay circuits and a related apparatus, and more particularly, to delay circuits and a related apparatus for extending delay time with active feedback elements.

[0003] 2. Description of the Prior Art

[0004] In the modern information-oriented society, many data are processed, stored, and transmitted conveniently by electrical signals. Engineers are researching and developing various kinds of circuits of specific functions to meet different demands.

[0005] In modern circuits, the memory in which data can be written, read, and erased in a nonvolatile manner, like flash

memory, has become one of the most important non-volatile storage media. Please refer to Fig.1. Fig.1 is the function blocks of a conventional flash memory 10. The flash memory 10 comprises a control circuit 12, a memory array 14, a charge pump 18, a limiter 17, a transmission circuit 20, and a delay circuit 16.

[0006] Please refer to Fig.2 (and also Fig.1). Fig.2 illustrates a waveform timing diagram of each related signal when the flash memory 10 is programming and erasing data. The horizontal axis in Fig.2 represents time and the vertical axis represents the waveforms.

[0007] As shown in Fig.2, when control circuit 12 starts data-programming/data-erasing at the time point t_s , the signal S_p will transfer from level L to level H at the time t_s and trigger the charge pump 18 to charge to voltage V_a . The limiter 17 also triggered by the signal S_p limits the voltage V_a to a stable level V_A after the voltage V_a raises to this level. Meanwhile, the limiter 17 will trigger the delay circuit 16 with the signal S_i when the voltage V_a equals level V_A . According to the triggering signal S_i , the control circuit 12 will pass the voltage V_a , which is generated by the charge pump 18 and reaches the level high enough, through the transmission circuit 20 to the memory array

14 to program/erase data.

[0008] As shown in Fig.2, when the voltage V_a is increased to the level V_A at the time t_0 , the limiter will transfer the signal S_i from level L to level H at this time, triggering the flash memory 10 to program/erase data and starting operation of the delay circuit 16. When the delay circuit 16 senses the change of the input signal S_i , it changes the signal level S_o after a predetermined time delay T_D . As shown in Fig.2, when the delay circuit 16 is triggered by the level change of the signal S_i at the time t_0 , after a delay time T_D , the output signal S_o will transfer from level L to level H at the time t_1 . The delay time T_D is the time for the flash memory 10 to complete data-programming/data-erasing. According to the level change of the signal S_o at the time t_1 , it makes sure that the control circuit 12 has enough time to complete data-programming/data-erasing.

[0009] As known by those skilled in the art, for the application described above, the delay time involved in the delay circuit 16 is generally about several μs ($1\mu s$ is one millionth of a second) to several ms ($1ms$ is one thousandth of a second), and even up to 100ms. However, the ordinary logic delay circuits often have a delay time of several ns

(1ns is one billionth of a second) and these ordinary logic cells can hardly be used as the delay circuit 16 in the flash memory 10. In order to meet the requirement of the specific control mechanism of data-processing in the flash memory, the delay circuit 16 in the flash memory 10 has to be designed with special consideration.

[0010] Please refer to Fig.3. Fig.3 shows a conventional delay circuit 22. The delay circuit 16 is biased between the DC voltages V_s and V_g . A voltage signal V_i is taken as an input and a voltage signal V_o is taken as an output. To implement the delay circuit 16 in Fig.1, the delay circuit 22 includes a p-type MOSFET M_{p0} , an n-type MOSFET M_{n0} , a resistor R , a capacitor C and an inverter I_0 . Gates of the transistors M_{p0} and M_{n0} are connected to node N_1 to receive the input signal V_i ; drains of the transistors M_{p0} and M_{n0} are connected to node N_2 , and the resistor R and the capacitor C are connected to node N_3 . The inverter I_0 inverts the voltage V_c of node N_3 to the voltage signal V_o as the output of the delay circuit.

[0011] As known from the above description, the delay time of the conventional delay circuit in Fig.3 is the time that it needs to discharge the capacitor C through the resistor R by the current I_n ; this time is proportional to the multipli-

cation of the capacitance and the resistance. In other words, to implement the long time delay of the delay circuit 16 in Fig.3, capacitance and resistance should be increased. This is one of the disadvantages of the conventional delay circuit. Large capacitance and large resistance require large layout area, so the layout area of the conventional delay circuit 22 cannot be reduced, increasing the production cost.

[0012] Please refer to Fig.4. Fig.4 is a conventional delay circuit 24, which is disclosed in United States Patent No. 5,969,557. It receives a voltage signal V_{pi} as input and produces a voltage signal V_{po} as output. The delay circuit 24 comprises a current generator 26, a voltage generator 28, a capacitor C_0 for the storage unit and a differential amplifier A_p . The current generator 26 includes p-type MOSFETs M_{p1} to M_{p3} . MOSFETs M_{p2} and M_{p3} form a current mirror to generate two current I_{r0} , I_{c0} of a specific ratio. A source and a drain of the transistor M_{p1} are connected to the DC bias V_s and the node N_{p2} , respectively, and a gate is controlled by the signal V_{pi} . The voltage generator 28 includes n-type MOSFETs M_{n1} and M_{n2} . A drain of the transistor M_{n1} is connected to the node N_{p2} by the resistor R_0 , a source is biased at the DC voltage V_g ,

and a gate is controlled by the signal V_{pi} . A drain and a source of the transistor M_{n2} are connected to the nodes N_{p3} and the DC bias V_g , respectively. A gate is controlled by the inverted signal V_{pi} of the inverter IP_0 . The positive and the negative ends of the differential amplifier A_p (marked as " + " and " - " in Fig.4) are connected to the nodes N_{p3} and N_{p2} respectively. This differential amplifier receives the voltages V_{pc} and V_{pr} as inputs and produces signal V_{po} as output.

[0013] As for the operation of the conventional delay circuit 24, please refer to Fig.5 (and also Fig.4). Fig.5 illustrates a waveform timing diagram of each voltage signal in the operation of the delay circuit 24 in Fig.4. The x-axis represents time and the y-axis represents voltage magnitude. As shown in Fig.5, when the input signal V_{pi} maintains the level L (as before the time t_{p0}), the transistor M_{p1} is turned on and makes the transistors M_{p2} and M_{p3} turn off. The turned-on transistor M_{p1} will keep the voltage V_{pr} of the node N_{p2} in the level H (like the level of the DC bias V_s), and the turned-on transistor M_{n2} keeps the voltage V_{pc} of the node N_{p3} in the level L (like the DC voltage V_g of the ground). Because the voltage levels V_{pc} and V_{pr} , which are positive and negative inputs of the

amplifier A_p , are L and H respectively, the output signal V_{po} of the amplifier A_p before time t_{p0} will maintain the level L , as shown in Fig.5.

[0014] At the time point t_{p0} , the input signal V_{pi} increases to the level H from the level L , triggering the function of the delay circuit 24. When the signal V_{pi} reaches the level H at t_{p0} , the transistor M_{p1} turns off and the transistor M_{n1} turns on. The turned-off transistor M_{p1} makes the transistors of the current mirror M_{p2} and M_{p3} turn on and generate the current of a fixed ratio I_{r0} and I_{c0} . In this situation, the current I_{r0} is the reference current passing through the resistor R_0 and generating a reference voltage V_{pr} with a stable level V_R at the node N_{p2} , as the voltage V_{pr} shows in Fig.5. The current I_{c0} is taken as a charging current, which charges the capacitor C_0 through the node N_{p3} to gradually increase the voltage V_{pc} of the node N_{p3} . As shown in Fig.5, at the time point t_{p1} , the voltage V_{pc} charged by the current I_{c0} increases to more than the level V_R , and the voltage V_{pc} of the positive input of the amplifier A_p is larger than that of negative input V_{pr} so that the output signal V_{po} of the amplifier A_p becomes the level H at time t_{p1} . In other words, the conventional delay circuit 24 delays the level change of the input

signal V_{pi} at time tp_0 to the level change of the output signal V_{po} at time tp_1 in order to implement the delay circuit. Time Td_0 between time points tp_0 and tp_1 is the delay time involved in the conventional delay circuit 24.

[0015] Compared to the delay circuit 22 in Fig.3, the delay circuit 24 in Fig.4 implements the function of delay by charging the capacitor C_0 directly with current I_{c0} so that it reduces the layout area, which RC circuits of the delay circuit 22 occupy. However, the delay circuit 24 in Fig.4 still has other disadvantages. First, the current mirror in the delay circuit 24 charges the capacitor C_0 with a constant current I_{c0} , so the voltage of the capacitor V_{pc} will increase rapidly with time in a fixed speed during the period of charging, as shown in Fig.5. Because the speed in which the fixed current I_{c0} charges the capacitor C_0 is too fast, it is hard to generate a long delay in the delay circuit 24. In addition, as shown in Fig.5, when the voltage V_{pc} of the capacitor C_0 is charged to the level V_R at time tp_1 , current I_{c0} will keep charging C_0 until the time point tp_2 when the voltage V_{pc} reaches the DC level V_s due to the characteristic of the delay circuit 24. In other words, even at time tp_1 when the delay circuit completes the function of the delay, current mirror of the conventional delay cir-

cuit 24 still consumes extra power to charge the capacitor C0, resulting in waste of power.

SUMMARY OF INVENTION

[0016] According to the claimed invention, a delay circuit is proposed for providing an output signal according to an input signal so that when the level of the input signal changes from a first input level to a second input level, the level of the output signal changes from a first output level to a second output level after a predetermined delay time. The delay circuit includes a voltage generator for providing a reference voltage when the input signal changes from the first input level to the second input level and a current generator for providing a charging current when the input signal changes from the first input level to the second input level. The delay circuit includes a feedback control module having a control end and two transmit ends, the control end for receiving a control signal, and the feedback control module able to transmit the charging current from the current generator between the two transmit ends, and the feedback control module changing the proportion between a cross voltage of the two transmit ends and the current between the two transmit ends. A storage unit is electrically connected to the

current generator for receiving the charging current from the feedback control module and generating a corresponding charging voltage. A feedback circuit is electrically connected between the storage unit and the control end of the feedback control module to provide the control signal according to the charging voltage. The delay circuit also includes an amplifier having two input ends electrically connected to the storage unit and the current generator in order to receive respectively the reference voltage and the charging voltage, the amplifier able to change the level of the output signal from the first output level to the second output level when the relationship between the reference voltage and the charging voltage changes.

[0017] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

BRIEF DESCRIPTION OF DRAWINGS

[0018] Fig.1 illustrates function blocks of a conventional flash memory.

[0019] Fig.2 illustrates a waveform timing diagrams of each relative signal when the flash memory in Fig.1 is program-

ming and erasing data.

[0020] Fig.3 illustrates a conventional delay circuit.

[0021] Fig.4 illustrates another conventional delay circuit.

[0022] Fig.5 illustrates a waveform timing diagram of each relative signal when the delay circuit in Fig.4 is operating.

[0023] Fig.6 illustrates function blocks of the delay circuit of the present invention.

[0024] Fig.7 illustrates a first embodiment of the delay circuit of the present invention.

[0025] Fig.8 illustrates a waveform timing diagram of each relative signal when the delay circuit in Fig.7 is operating.

[0026] Fig.9 illustrates a second embodiment of the delay circuit of the present invention.

[0027] Fig.10 illustrates a waveform timing diagram of each relative signal when the delay circuit in Fig.9 is operating.

[0028] Fig.11 illustrates a third embodiment of the delay circuit of the present invention.

[0029] Fig.12 illustrates a waveform timing diagram of each relative signal when the delay circuit in Fig.11 is operating.

[0030] Fig.13 illustrates a fourth embodiment of the delay circuit of the present invention.

[0031] Fig.14 illustrates a waveform timing diagram of each rela-

tive signal when the delay circuit in Fig.13 is operating.

DETAILED DESCRIPTION

[0032] In prior art, the method for implementing the delay function of the delay circuit is through charging or discharging with RC circuits or a fixed current. However, these conventional methods require larger layout area and are hard to generate a long period of delay time.

[0033] The delay circuit of the present invention comprises a current generator, a voltage generator, a storage unit (like a capacitor), a feedback control module formed by active devices, and a differential amplifier. When the level of the input signal changes and triggers functions of the delay circuit, the voltage generator generates a reference voltage and the current generator generates a reference current. Then the feedback control module passes the charging current to the storage unit to do charging or discharging, and increases or decreases the output voltage of the storage unit. The amplifier is used to compare the charging voltage and the reference voltage. When the comparison result between the charging voltage and the reference voltage changes, the amplifier triggers the level of the output signal to implement the function of delay. During the period of charging or discharging storage unit, when

the charging voltage is close to the reference voltage, the feedback control module will dynamically decrease the charging current passed to the storage unit, leading to the slower speed in which the charging voltage approaches the reference voltage. Therefore, the delay circuit of the present invention can prolong the delay time effectively. In addition, the feedback control module is composed of active devices (like transistors) and can reduce the large layout area of the RC circuits.

[0034] Please refer to Fig.6. Fig.6 illustrates function blocks of the delay circuit 30 in the present invention. The delay circuit 30 receives the signal $Si0$ as input and outputs the signal $So0$. It transforms the level change of the signal $Si0$ to the level change of the signal $So0$ after a delay time. The delay circuit 30 has a voltage generator 32A, a current generator 32B, a feedback control module 34A, a feedback circuit 34B, a storage unit 36, and a differential amplifier Am .

[0035] When the level of the signal $Si0$ changes and triggers functions of the delay circuit 30, the voltage generator 32A generates a reference voltage Vr and the current generator 32B generates a reference current Ic . Then the feedback control module passes the charging current Ic to

the storage unit 36 through the feedback control module 34A. The storage unit 36, which can be implemented by a capacitor, provides a charging voltage V_{c0} according to the charging or discharging of current I_c . The charging voltage V_{c0} will be passed to the feedback circuit 34B and the amplifier A_m . The feedback circuit 34 produces a control signal S_c by the charging voltage V_{c0} and this control signal S_c will feedback to a control end 37C in the control module 34A. The feedback control module 34A can dynamically adjust the charging current I_c passed to the storage unit 36 according to the control signal S_c . At the same time, the amplifier keeps comparing the charging voltage V_{c0} and the reference voltage V_r . When the comparison result between the charging voltage V_{c0} and the reference voltage V_r changes during the period when the charging voltage is close to the reference voltage, the amplifier is triggered to change the level of the output signal S_{o0} to implement the function of delay.

[0036] One of the characteristics of the present invention is that the feedback control module 34A dynamically adjusts the charging current I_c passed to the storage unit 36. In practical operation, when the current generator 32B provides the charging current I_c and gradually changes the charg-

ing voltage V_{c0} of the storage unit 36, the feedback circuit 34 changes the control signal Sc according to the charging voltage V_{c0} . The feedback control module 34A senses that the charging voltage V_{c0} is close to the reference voltage V_r by the control signal Sc , and it will gradually decrease the charging current I_c passed to the storage unit 36, making slower the speed in which the charging voltage approaches the reference voltage. The time when the charging voltage V_{c0} reaches the reference voltage V_r is extended, and thus the delay circuit 30 implements a longer delay time. In the preferred embodiment of the present invention, the feedback control module is composed of active devices (like transistors) and can reduce the large layout area of the RC circuits.

[0037] Please refer to Fig.7. Fig.7 is a first embodiment of the delay circuit 40. The delay circuit 40 receives a voltage signal V_{i1} as input and produces a voltage signal V_{o1} as the outputs after delay. In the delay circuit 40, the resistor R_{a1} , R_{a2} and an n-type MOSFET Q_{n1} form a voltage divider to implement the voltage generator 32A and produce a reference voltage V_{r1} at the node $Na2$. Gate of the transistor Q_{n1} receives the trigger signal V_{i1} at the node $Na1$. P-type MOSFET Q_{p2} , n-type MOSFET Q_{n2} , the in-

verter I1 form a current generator 42B, which generates a charging current I_{c1} from the source and drain of the transistor Qp2. P-type MOSFET Qp1 is the feedback control module in the present invention. Gate is the control end, while drain and source, connected to the DC bias V_s and drain of the transistor Qp2 respectively, are transition ends. The transistor Qp1 controls the current I_{c1} of the current generator 42B. The capacitor C_a , the storage unit of the delay circuit 40, receives the current I_{c1} at the node Na3 to produce a charging voltage V_{c1} at the node Na3. The connection between the node Na3 and gate of the transistor Qp1 forms a feedback circuit, which feeds back the voltage V_{c1} to the control end of the transistor Qp1. The positive and negative inputs of the amplifier A1 (marked as " + " and " - " in Fig.7) receive the voltage V_{c1} and V_{r1} respectively, and generate voltage signal V_{o1} as the output signal of the delay circuit 40.

[0038] As for the operation of the delay circuit 40, please refer to Fig.8(also Fig.7). Fig.8 illustrates a waveform timing diagram of each voltage signal in the operation of the delay circuit 40 in Fig.7. The x-axis represents time and the y-axis represents voltage magnitude. As shown in Fig.8, before time t_{a0} , input signal V_{i1} maintains the level L, and

the transistor Qn1 in the voltage generator 42A is off. The voltage of the resistor Ra1 is zero, keeping the voltage Vr1 in the DC level H like the voltage. Because the input signal Vi1 is in the level L, the inverted level H makes the transistor Qn2 of the current generator 42B turn on and pull the charging voltage Vc3 of the node Na3 to the level L. The reference voltage Vr1 maintaining the level H makes the transistor Qp2 off. Because voltage Vr1 is larger than voltage Vc1, the output signal Vo1 of the amplifier A1 maintains the level L.

[0039] At time ta0, input signal Vi1 transfers from the level L to the level H and starts triggering functions of the delay circuit 40. The signal Vi1 in the level H makes the transistor Qn1 in the voltage generator 42A conduct current, passing through the resistors Ra1, Ra2 and producing the stable DC voltage Vs at the node Na2. As shown in Fig.8, after time ta0, the reference voltage Vr1 maintains the level V1, which is about $V_s \cdot R_{a2} / (R_{a1} + R_{a2})$. After time ta0, input signal Vi1, which has transferred to the level H, makes the transistor Qn2 in the current generator 42B turn off. Accordingly, the transistors Qp2, Qp1 turn on, letting the charging current enter capacitor Ca through the node Na3 to charge the capacitor Ca. Meanwhile, voltage Vc1 at the

node Na3 begins to increase at time t_{a0} , as shown in Fig.8. Voltage V_{c1} reaches or even goes beyond the level V_1 of the voltage V_{r1} until time t_{a2} . The output signal V_{o1} of the amplifier A1 will transfer from the level L to the level H because the voltage V_{c1} is larger than V_{r1} at this time. In other words, the delay circuit 40 delays the level change of the input signal V_{i1} at time t_{a0} for time T_{d1} (as shown in Fig.8), and responds with the level change of output signal V_{o1} at time t_{a2} , achieving the function of delay.

[0040] As described before, one characteristic of the present invention is that the feedback control module decreases the charging current dynamically when charging/discharging the storage unit so as to lengthen the delay time. In the delay circuit 40, gate voltage of the transistor Qp1 in the feedback control module increases with the increase of the voltage V_{c1} after time t_{a0} . This makes the voltage between the source and gate of the transistor Qp1 decrease, and weakens conducting of the transistor Qp1. Accordingly, the current I_{c1} entering the node Na3 in the current generator 42A gradually decreases, slowing down the increase of the voltage V_{c1} . As shown in Fig.8, waveform of voltage V_{c1} after time t_{a0} shows a concave decreasing

curve, which means the increasing speed (that is the slope of the curve) becomes slower with time. Thus, it needs more time for voltage V_{c1} to accumulate to the level V_1 .

The present invention is based on this origin to implement the longer delay of the delay circuit. The transistor Q_{p1} in the feedback control module is equivalent to a changeable resistor. The equivalent resistor between source and drain changes dynamically with the gate voltage V_{c1} and decreases conducting current I_{c1} dynamically.

[0041] To describe the effect of the present invention, Fig.8 shows the voltage waveform V_{c1s} of the dotted line when voltage V_{c1} increases if the circuit excludes the transistor Q_{p1} . Without the transistor Q_{p1} , the transistor Q_{p2} is a constant current source (like the current generator of the conventional delay circuit 24 in Fig.4). In this case, voltage V_{c1} will linearly increase rapidly, making voltage V_{c1} charge to the level V_1 and trigger the level change of output signal V_{o1} in the advanced time t_{a1} . Adding the transistor Q_{p1} for the feedback control module of the present invention decreases the charging current I_{c1} dynamically when the capacitor C_a is charging. It lengthens the time when voltage V_{c1} reaches the level V_1 effectively, and implements a delay circuit with more delay time than the

conventional delay circuit.

[0042] In addition, after adding the feedback control module in the present invention, the highest voltage level of the capacitor C_a is $(V_s - V_t)$ (V_t is threshold voltage the transistor Q_{p1}), due to the voltage between source and drain of the transistor Q_{p1} . This will decrease power consumption that the capacitor C_a needs for charging. Comparatively, the conventional delay circuit 24 in Fig.4 should charge the capacitor C_0 to the higher level, consuming more power.

[0043] Because the feedback control module in the present invention is implemented by active devices, say transistors, it occupies less layout area. The conventional resistor-capacitor delay circuit 22 in Fig.3 requires large layout area to implement the delay circuit with long delay. In addition, the delay circuit in the present invention can be reset rapidly. As shown in Fig.7 and Fig.8, if the input signal V_{i1} becomes level L from the level H at time t_{a2} and resets the delay circuit 40, input signal V_{i1} of the level L will turn on the transistor Q_{n2} by the high output level of the inverter I_1 , and the turned-on transistor Q_{n2} rapidly discharges the transistor C_a through the node N_{a3} directly. When the input signal V_{i1} is in the level L, both the transistor Q_{p2} and the transistor Q_{p1} serving as the feedback

control module are turned off, so they will not affect that the transistor Qn2 rapidly discharges the capacitor Ca. This also makes the delay circuit 40 in the present invention reset rapidly. Comparatively, the conventional delay circuit 22 in Fig.3 cannot reset signals rapidly for charging/discharging the capacitor through the resistor.

[0044] Please refer to Fig.9. Fig.9 illustrates another embodiment of the delay circuit 50 in the present invention. The delay circuit 50 takes voltage signal Vi2 as an input signal and voltage signal Vo2 as an output signal. In the delay circuit 50, p-type MOSFETs Qp5 to Qp7 and n-type MOSFET Qn6 form the current generator 52B, and gates of the transistors Qp5, Qp6 are connected together to form a current mirror. When the current generator 52B starts operating, the transistors Qp5, Qp6 conduct a current Ir2 and a charging current Ic2 respectively. An N-type MOSFET Qn5 and the resistor Rb compose a voltage generator 52A. When the transistor Qn5 turns on, the voltage generator 52A receives the reference current Ir2 provided by the current generator 52B at node Nb2, and produces a reference voltage Vr2 at the node Nb2. Source and drain of the N-type MOSFET Qn7 are connected together to form a capacitor, which is the storage unit of the delay circuit 50

and receives current I_{c2} from the node Nb3. Similarly, the delay circuit 50 of the present invention uses p-type MOSFET Qp8 as the feedback control module. Source and drain of the transistor Qp8 form two transmission ends to control current I_{c2} , and the gate connected at the node Nb3 receives voltage V_{c2} as the control signal to dynamically adjust the current I_{c2} . Positive and negative ends of the amplifier A2 in the delay circuit 50 receive voltage V_{c2} and V_{r2} respectively, and the output voltage signal V_{o2} is produced according to the relative magnitude of these two inputs.

[0045] Please refer to Fig.10 (also Fig.9). Fig.10 is a waveform timing diagram of each relative signal of the delay circuit 50 in Fig.9. The horizontal axis represents time and the vertical axis represents voltage magnitude. As shown in Fig.10, When the input signal V_{i2} maintains the level L before time t_{b0} , the on-transistor Qp7 and the off-transistor Qn5 will make the voltage V_{r2} at node Nb2 short and become close to the level H, and turn off the transistors Qp5, Qp6 in the current generator 52B. The turned-on transistor Qn6 pulls the voltage V_{c2} of the node Nb3 down to the level L. Because voltage V_{c2} and V_{r2} remain in the levels L and H respectively, output sig-

nal V_{o2} of the amplifier A2 will remain in the level L.

[0046] Input signal V_{i2} reaches the level H at time t_{b0} and triggers the delay circuit 50, turning on the transistor Q_{n5} and turning off the transistor Q_{p7} . Accordingly the transistor Q_{p5} , Q_{p6} and Q_{p8} turns on and provides currents I_{r2} , I_{c2} . The reference current I_{r2} will go through the resistor R_b and produce a stable voltage V_{r2} in the level v_2 at node N_{b2} (V_2 is almost equal to $I_{r2} \cdot R_b$). Charging current I_{c2} charges the storage unit, the transistor Q_{n7} , through the node N_{b3} , and the voltage V_{c2} at node N_{b3} increases from the level L. Similar to the operation of the delay circuit 40 in Fig.7, with the increase of the voltage at node N_{b3} , the transistor Q_{p8} as the feedback control module gradually leaves the turned-on mode, and current I_{c2} also starts decreasing. Thus, the speed in which the voltage V_{r2} increases is slower, and delay time becomes longer. At time t_{b2} , charging voltage V_{c2} goes beyond the level V_2 , and the amplifier A2 changes the signal V_{o2} from the level L to the level H. During the level change of the signal V_{i2} , V_{o2} , delay time T_{d2} is generated.

[0047] Similar to the delay circuit 40 in Fig.7, the highest voltage V_{c2} of the transistor Q_{p8} in the delay circuit 50 is $(V_s - V_t)$ due to the limit of threshold voltage (V_t is the threshold

voltage of the transistor Qp8). This decreases the power consumption of the delay circuit 50. When the input signal Vi2 transfers from the level H to the level L to trigger the delay circuit 50, the transistor Qn7 as the storage unit can be discharged directly by the turned-on transistor Qn6 to complete resetting rapidly. In other words, the delay circuit 50 and the delay circuit 40 have the same advantages that the delay circuit with long delay can be implemented by smaller layout area. In the previous two examples of the present invention, the feedback control module is formed by p-type MOSFETs to combine with the current generator of p-type MOSFETs, for adjusting the charging current or discharging the storage unit. Meanwhile, the feedback control module triggers the delay circuit when the input signal transfers from the level L to the level H, produces delay time between input and output signals. Of course, the feedback control module of the present invention can also be implemented as an n-type MOSFET to combine the current generator of an n-type MOSFET. Moreover, the delay circuit can be designed to be triggered by the falling edge of the input signal. In these examples, please refer to Fig.11 and Fig.12. Fig.11 illustrates the delay circuit 60 of a third embodiment in the

present invention. Fig.12 is a waveform timing diagram of each relative signal of the delay circuit 60 in Fig.11. The horizontal axis represents time and the vertical axis represents voltage magnitude. The delay circuit 60 receives a voltage signal V_{i3} as an input signal, and outputs a voltage signal V_{o3} .

[0048] As shown in Fig.11, p-type MOSFET Q_{p8} and the resistors R_{e1} and R_{e2} form a voltage divider in the delay circuit 60, and is labeled as a voltage generator 62A, which provides the reference voltage V_{r3} at node N_{c2} . N-type MOSFET Q_{n10} and p-type MOSFET Q_{p10} form a current generator 62B. When the delay circuit 60 is in operation, the current generator 62B serves as the current source, producing a current I_{c3} from node N_{c3} to discharge the capacitor C_c . The capacitor C_c can be like a MOSCAP in Fig.9, serving as the storage unit in the delay circuit 60 so as to produce a discharging voltage V_{c3} at node N_{c3} . N-type MOSFET Q_{n9} is the feedback control module, and the gate receives the feedback signal, voltage V_{c3} , to control current I_{c3} . The amplifier A_3 compares the voltage V_{c3} and V_{r3} , by which the output voltage signal V_{o3} is produced.

[0049] As shown in Fig.12, the delay circuit 60 of the present invention in Fig.11 is triggered when input signal V_{i3} trans-

fers from the level H to the level L. Before time t_{c0} , input signal V_{i3} maintains the level H, and the transistor Q_{p8} is off. The voltage of the resistor R_{e2} is zero, keeping the voltage V_{r3} in the level L like the ground voltage V_g .

Meanwhile, the signal V_{i3} of the level L is fed into the inverter I_3 and the transistor Q_{p1} is turned on. In the situation where transistor Q_{n10} is off, the voltage at node N_{c3} is pushed to the level H of the bias voltage V_s . Because two input voltages V_{c3} and V_{r3} of the amplifier A_3 are in the level H and L respectively, output signal V_{o3} remains in the level H, as shown in Fig.12.

[0050] Input signal V_{i3} transfers from the level H to the level L at time t_{c0} and triggers the delay circuit 60, turning on the transistor Q_{p8} . R_{e1} and R_{e2} divide the voltage V_s , and the voltage V_{r3} becomes the level V_3 (as shown in Fig.12; voltage level V_3 approximately equals $V_s \cdot R_{e2} / (R_{e1} + R_{e2})$). Meanwhile, signal V_{i3} in the level L is input in the inverter I_3 and then turns off the transistor Q_{p10} . The on-transistor Q_{n10} and Q_{n9} discharges the capacitor C_c by current I_{c3} . As shown in Fig.12, voltage V_{c3} decreases after time t_{c0} when current I_{c3} discharges the capacitor. In addition, the transistor Q_{n9} as the feedback control module gradually leaves the turned-on mode because the gate

voltage V_{c3} decreases, and current I_{c3} also decreases. Thus, the speed in which the capacitor C_c is discharged is slower, and time for voltage V_{c3} to decrease becomes longer. At time t_{c2} , voltage V_{c3} becomes lower than voltage V_{r3} , so the output signal V_{o3} of the amplifier A_3 transfers from the level H to the level L due to change of the relative magnitude of V_{c3} and V_{r3} . In summary, input signal V_{i3} changes the level at time t_{c0} , and after a delay time output signal V_{o3} in the delay circuit 60 at time t_{c2} changes its level. T_{d3} between time t_{c0} and time t_{c2} is the delay time generated by the delay circuit 60.

[0051] As known from the description above, the delay circuit 60 of the present invention dynamically decreases current I_{c3} when voltage V_{c3} of the transistor Q_{n9} gradually leaves the turned-on mode. Thus, it takes longer for voltage V_{c3} to decrease to the level V_3 of voltage V_{r3} , and implement the delay circuit of longer delay. Without the transistor Q_{n9} , the transistor Q_{n10} becomes a current source, which discharges capacitor C_c with stable current I_{c3} . In this situation, voltage V_{c3} will linearly decrease rapidly. Fig.12 shows the voltage waveform V_{c3s} of the dotted line when voltage V_{c3} decreases rapidly if the circuit excludes the transistor Q_{n9} . Voltage V_{c3} will decrease to the level of

voltage V_{r3} at time t_{c1} , and the output signal V_{o3} of the amplifier A3 changes to the level L from the level H at the advanced time t_{c1} . Thus it can be seen that in the present invention with the feedback control of the current I_{c3} by the transistor Qn9, the delay circuit 60 lengthens the delay time rapidly. In addition, the feedback control module in the present invention limits the lower bound which voltage V_{c3} decreases to, making the capacitor Cc discharge to $(V_g + V_t)$ at most, of which V_t is threshold voltage of transistor Qn9. Therefore, the delay circuit 60 of the present invention consumes less power. In comparison, to bias the source of the transistor Qn10 at the DC voltage V_g without transistor Qn9, the level of voltage V_{c3} will keep decreasing until it arrives at the level L, as voltage V_{c3s} shows in Fig.12. This wastes more power when discharging.

[0052] Please refer to Fig.13 and Fig.14. Similar to the embodiment of the present invention in Fig.9, the present invention can be implemented by a current mirror with n-type MOSFETs. Fig.13 illustrates another embodiment of the delay circuit 70 in the present invention. Fig.14 shows a waveform timing diagram of relative signals of the delay circuit 70. The x-axis represents time and the y-axis rep-

resents voltage magnitude of the waveform. The delay circuit 70 takes a voltage signal V_{i4} as input signal, and when signal V_{i4} transfers from the level H to the level L, it triggers the delay circuit 70 and outputs a voltage signal V_{o4} .

[0053] As shown in Fig.13, the voltage generator 72A of the delay circuit 70 is composed of a p-type MOSFET Q_{p13} as well as a resistor R_d , and generates a reference voltage V_{r4} at node Nd2. N-type MOSFETs Q_{n13} and Q_{n14} , which are similar to a current mirror, and n-type MOSFET Q_{n12} form the current generator 72B. When the current generator 72B operates, transistors Q_{n13} and Q_{n14} conduct current I_{r4} and current I_{c4} respectively as a reference and a discharging current. A source and a drain of the N-type MOSFET Q_{n15} (it can also be a p-type MOSFET) are connected together to form a MOSCAP, serving as the storage unit of the delay circuit 70 and generating the voltage V_{c4} at node Nd4 for serving as a discharging voltage. An N-type MOSFET Q_{n11} as the feedback control module controls current I_{c4} by the signal fed back to the gate of MOSFET Q_{n11} . Positive and negative inputs of the amplifier A4 receive voltage V_{r4} and V_{c4} respectively and decide the level of output signal V_{o4} by their relative magni-

tude.

[0054] As shown in Fig.14, when input signal V_{i4} maintains the level H before time t_{d0} , transistor Q_{n12} turns on and makes transistors Q_{n13} and Q_{n14} turn off, resulting in the level L of the voltage V_{r4} at node $Nd2$. Meanwhile, through the inverter $I4$, signal V_{i4} of the level H also turns on the transistor Q_{p14} , leading to the level H of the voltage V_{c4} at node $Nd4$. Because the voltage V_{c4} in the level H is larger than the voltage V_{r4} in the level L, the amplifier $A4$ keeps the output signal V_{o4} in the level H.

[0055] Input signal V_{i4} transfers from the level H to the level L at time t_{d0} and triggers the delay circuit 40, turning off the transistor Q_{n12} . Accompanied with the turned-on transistor Q_{p13} , transistors Q_{n13} and Q_{n14} conduct current I_{r4} and I_{c4} respectively. The current I_{r4} , which flows through the resistor R_d , produces a voltage V_{r4} of the level V4 (voltage level V4 approximately equals $V_s - I_{r4} \cdot R_d$). Meanwhile, with the off-transistor Q_{p14} , current I_{c4} discharges the storage unit, formed by the transistor Q_{n15} , and the voltage V_{c4} at node $Nd3$ decreases from the level H. During the decrease of the voltage V_{c4} , the transistor Q_{n11} the gate of which is controlled by voltage V_{c4} gradually leaves the turned-on mode, and accordingly

current I_{c4} decreases, retarding the decrease of the voltage V_{c4} . At time t_{d2} , voltage V_{c4} falls below the level V_4 of the voltage V_{r4} , and the amplifier A_4 changes the signal V_{o4} from the level H to the level L. T_{d4} generated between the signal V_{i4} and V_{o4} is the delay time.

[0056] Similar to the embodiment of the present invention in Fig.9, the embodiment 70 has longer delay, lower power consumption and fast resetting.

[0057] The delay circuit of the present invention generates delay in the following mechanism. A current generating circuit triggered by the level change of the input signal generates a current to charge or discharge the storage unit. Then, an amplifier compares the charging voltage generated by the storage unit and the reference voltage produced by the voltage generator. When the relative magnitude of charging voltage and reference voltage changes, the level of the output signal also changes. The delay time is therefore generated between the level change of the input signal and output signal. When the level of charging voltage approaches the level of reference voltage, the feedback control module of the present invention will dynamically decrease the charging/discharging current passed to the storage unit by the current transmission circuit, slowing

the speed in which charging voltage reaches the reference voltage so as to implement a longer delay. Compared to the conventional resistor–capacitor delay circuit, or the conventional delay circuit with fixed charging current source, the delay circuit of the present invention consumes less power and implement a longer delay with smaller layout area. Delay circuits of the present invention used in the flash memory can reduce the total chip area of the flash memory, and generate enough delay time for the flash memory to do data–programming/data–erasing so that the flash memory will operate correctly.

[0058] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.